IN THE CLAIMS

1. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a service class identifier.

2. (Canceled)

3. (Previously Presented) The network switch of claim 1 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

4-5. (Canceled)

6. (Original) The network switch of claim 3 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

7. (Original) The network switch of claim 3 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

8. (Original) The network switch of claim 3 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

9. (Previously Presented) The network switch of claim 1 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

10. (Original) The network switch of claim 3 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

11-18. (Canceled)

19. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress cards segregates incoming data into queues based on a service class identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

20. (Original) The network switch of claim 19 wherein N and M are equal.

21. (Canceled)

22. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the ingress interfaces segregates incoming data into queues based on a flow identifier.

23. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a user identifier.

24. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a session identifier.

25. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a quality of service (QoS) identifier.

26. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a priority identifier.

27. (Previously Presented) A network switch having an asynchronous mesh to transfer data from ingress interfaces to egress interfaces, the ingress interfaces to receive data from external sources and to selectively schedule and asynchronously transmit the data across the asynchronous mesh to the egress interfaces, the egress interfaces to receive data from the asynchronous mesh and to schedule and transmit the data to external destinations, wherein one or more of the N ingress interfaces segregates incoming data into queues based on a deadline identifier.

28. (Canceled)

29. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein

one or more of the ingress cards segregates incoming data into queues based on a flow identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

30. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress cards ~~interfaces~~ segregates incoming data into queues based on a user identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

31. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress cards segregates incoming data into queues based on a session identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

32. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress cards segregates incoming data into queues based on a quality of service (QoS) identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the

egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

33. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress cards segregates incoming data into queues based on a priority identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

34. (Previously Presented) A network switch comprising:

N ingress cards coupled to receive data from external sources, the N ingress cards having a plurality of ports to transmit data, wherein each of the N ingress cards comprises an ingress scheduler coupled to the ports of the ingress card, the ingress scheduler to cause data to be selectively and asynchronously transmitted via the ports of the ingress card, and further wherein one or more of the ingress interfaces segregates incoming data into queues based on a deadline identifier; and

M egress cards having ports coupled to receive data from one or more of the plurality of ports of the N ingress cards, the egress cards coupled to transmit data to external destinations, wherein each of the M egress cards comprises an egress scheduler coupled to the ports of the egress card, the egress scheduler to cause data to be selectively transmitted to the external destinations.

35. (Canceled)

36. (Previously Presented) The network switch of claim 22 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

37. (Previously Presented) The network switch of claim 36 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

38. (Previously Presented) The network switch of claim 36 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

39. (Previously Presented) The network switch of claim 36 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

40. (Previously Presented) The network switch of claim 22 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

41. (Previously Presented) The network switch of claim 36 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

42. (Previously Presented) The network switch of claim 23 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

43. (Previously Presented) The network switch of claim 42 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

44. (Previously Presented) The network switch of claim 42 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

45. (Previously Presented) The network switch of claim 42 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

46. (Previously Presented) The network switch of claim 23 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

47. (Previously Presented) The network switch of claim 42 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

48. (Previously Presented) The network switch of claim 24 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache

buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

49. (Previously Presented) The network switch of claim 48 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

50. (Previously Presented) The network switch of claim 48 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

51. (Previously Presented) The network switch of claim 48 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

52. (Previously Presented) The network switch of claim 24 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

53. (Previously Presented) The network switch of claim 48 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

54. (Previously Presented) The network switch of claim 25 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

55. (Previously Presented) The network switch of claim 54 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

56. (Previously Presented) The network switch of claim 54 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

57. (Previously Presented) The network switch of claim 54 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

58. (Previously Presented) The network switch of claim 25 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

59. (Previously Presented) The network switch of claim 54 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

60. (Previously Presented) The network switch of claim 26 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

61. (Previously Presented) The network switch of claim 60 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

62. (Previously Presented) The network switch of claim 60 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

63. (Previously Presented) The network switch of claim 60 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

64. (Previously Presented) The network switch of claim 26 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

65. (Previously Presented) The network switch of claim 60 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

66. (Previously Presented) The network switch of claim 27 comprising N egress interfaces, each of the egress interfaces further comprising N independent cache buffers coupled to N respective ingress interfaces to receive data from the respective N ingress interfaces and further comprising N ingress interfaces, each of the N ingress interfaces having N independent cache buffers, each of the N independent cache buffers coupled to one of N respective egress interfaces.

67. (Previously Presented) The network switch of claim 66 in which the egress interfaces generate a flow control signal to prevent access to one or more of the N buffers of the respective egress interfaces.

68. (Previously Presented) The network switch of claim 66 wherein the egress interfaces generate a flow control signal to prevent transmission to one or more of the N buffers of the respective egress interfaces.

69. (Previously Presented) The network switch of claim 66 wherein the N ingress interfaces transfer data to a shared egress buffer and further wherein the egress interfaces schedule and retrieve the data stored in the shared egress buffer prior to transmitting the data to the external destinations.

70. (Previously Presented) The network switch of claim 27 in which the egress interfaces generate a flow control signal to prevent access by one or more of the queues at the ingress interfaces to the egress buffer.

71. (Previously Presented) The network switch of claim 66 in which the N ingress interfaces concurrently transmit fixed-length cells and variable-length packets across the mesh to the egress interfaces.

72. (Previously Presented) The network switch of claim 29 wherein N and M are equal.

73. (Previously Presented) The network switch of claim 30 wherein N and M are equal.

74. (Previously Presented) The network switch of claim 31 wherein N and M are equal.

75. (Previously Presented) The network switch of claim 32 wherein N and M are equal.

76. (Previously Presented) The network switch of claim 33 wherein N and M are equal.

77. (Previously Presented) The network switch of claim 34 wherein N and M are equal.